Design of a 5 kV, 2 kW Series-loaded Resonant Power Converter

By Marco Denicolai

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1. ABSTRACT

A solid-state Series-loaded Resonant (SLR) Power Converter has been designed and built as a module of a bigger CCPS (Capacitor-Charging Power Supply). The converter is based on a series-loaded resonant topology and uses IGTBs as switching devices: it is capable of charging a 0.1 μF capacitor up to 5 kV in 0.6 ms time. This accounts for a charging power of 2 kJ/s.

An improved immunity to transients and noise has been reached as a result of an extensive investigation and tackling of all encountered failure modes.

2. INTRODUCTION

A medium-sized Tesla transformer is under construction at the HUT High Voltage Laboratory: its primary circuit features a 100 μH inductor and a 0.1 μF capacitor. This capacitor has to be charged to a voltage variable between 5 to 20 kV, to be successively discharged on the inductor producing a high current peak and, consequently, a high pulsed magnetic field. The capacitor discharge is performed through a rotating spark gap that can achieve a maximum break rate of 400 Hz: the spark gap is connected in parallel to the power supply output, thus short-circuiting it when conducting (Figure 2.1).

The requirements for a power supply charging the Tesla transformer capacitor are severe:

- Charging voltage regulated from 5 to 20 kV DC.
- Charging time as low as 2.5 ms (for a 400 Hz break rate)
- Capacity to withstand shortcircuits
- Capacity to withstand high-voltage transients of positive and negative polarity.

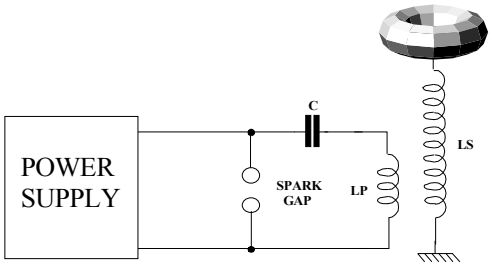

Figure 2.1 Basic schematic of a Tesla transformer.

The required charging voltage, together with the constraint of the charging time, translates into a required maximum power of 8 kW. The difficulty to reliably control such a power at the high-voltage side practically forbids any approach featuring a more or less stabilized DC high-voltage to be generated from a conventional 50 Hz transformer through rectification.

Instead, it is more attractive to utilize a high-frequency converter performing the regulation at the low-voltage side of its step-up transformer and charging the primary capacitor with high voltage pulses. Such a device is not capable of providing a stabilized DC voltage and, therefore, can be merely regarded as a Capacitor-Charging Power Supply (CCPS).

3. POWER SUPPLY ARCHITECTURE

A scalable, modular architecture allows simplifying the problem of the construction of the 20 kV 8 kW step-up transformer and the selection of electronic components suitable to drive it. A subdivision of the power supply into four identical blocks reduces the requirements to four 5 kV 2 kW modules, which can be implemented with off-the-self components. The outputs of the four modules are then connected in series to provide the full operational voltage (Figure 3.2).

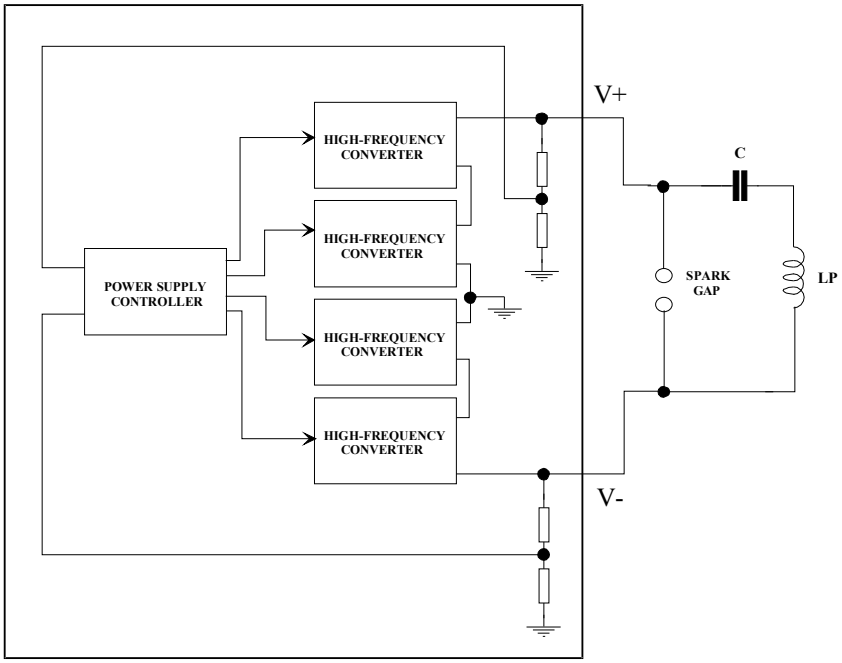

Figure 3.2 Power supply architecture.

The design is scalable, as more converter modules can be added in series to reach a higher charging voltage, being their output floating in respect to ground. The CCPS output is internally center-tapped to ground: one of the output leads, therefore, assumes a maximum potential of +10 kV while the other one assumes a minimum potential of –10 kV (in respect to ground). This strategy increases safety and allows to reduce to one half (10 kV DC) the insulation requirements of assemblies and wiring.

The converter modules are fed with 560 V DC obtained by rectifying 400 V AC from the mains (Figure 3.3). A full-bridge switch drives a step-up transformer with a 9:1 turns ratio in order to reach a rectified output voltage of about 5 kV DC. A single controller module samples the charging voltage and drives the converters: it is responsible of synchronizing the charge with external events and suspending the charging pulses when a predetermined voltage is reached. Galvanic isolation is arranged at the converter drive inputs in order to reduce noise and interference propagation

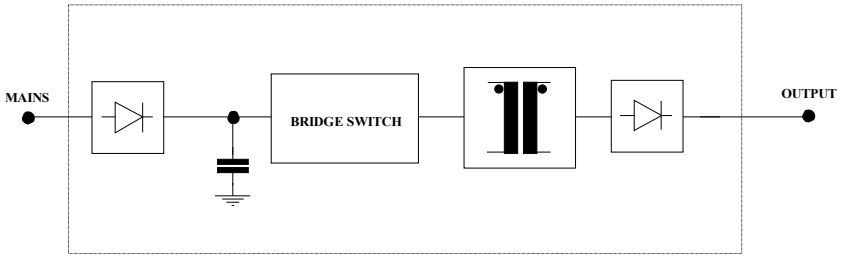

Figure 3.3 Basic block diagram of one converter module.

4. SLR THEORY OF OPERATION

The topology selected for the converter is the series-loaded resonant [Moh89, Lip91, Nel90]. In this configuration (Figure 4.4) the switches and resonant components L and C are connected to the low voltage side of the transformer: only the rectifiers on the transformer secondary must have high voltage ratings. By closing in proper order the switches in pairs, pulses of alternate polarity are applied to the transformer: using a high turn ratio, high voltage pulses are generated at the secondary, increasing the capacitor charge. The characteristic impedance Z_0 of the bridge load is given by:

$$Z_0 = \sqrt{\frac{L}{C_{eq}}} \qquad \text{(Eq.1)}$$

And its resonance frequency f_0 by:

$$f_0 = \frac{1}{2\pi\sqrt{LC_{eq}}} \qquad \text{(Eq.2)}$$

C_{eq} is the series combination of capacitors C and C'$_c$, where C'$_c$ is the equivalent capacitance C_c reflected to the primary. For a 9:1 turn ratio is:

$$C_c' = \left(\frac{N_2}{N_1}\right)^2 C_c = 81 \cdot C_c \qquad \text{(Eq.3)}$$

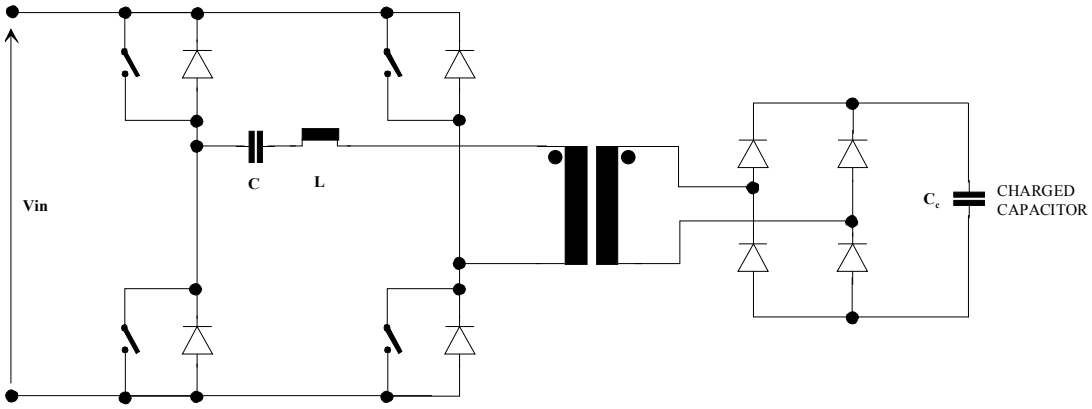

Figure 4.4. Series-loaded resonant converter.

As usually in high-voltage applications, C_c (0.1 μF in this case) is at least an order of magnitude greater than C. Then its contribute is negligible and:

$$C_{eq} = \frac{1}{\frac{1}{C} + \frac{1}{C_c'}} \approx C \qquad \text{(Eq.4)}$$

Therefore, Z_0 and f_0 are uniquely defined by C and L. Operating the circuit at a frequency $f_s < f_0/2$, all switches and anti-parallel diodes turn on and off at zero current. Using a frequency $f_0/2 < f_s < f_0$ the diodes' turn off and the switches' turn on happens at a current greater than zero. Conversely, for $f_s > f_0$, the diodes turn on and the switches turn off at a current greater than zero. Operation at a frequency slightly less than $f_0/2$ presents several advantages:

- Because the commutation of switches and diodes happens when the current is zero, switching losses are reduced to a minimum and no snubbers are required
- For the same reason, switch commutation time and diode reverse recovery time are not critical
- At this frequency (or at a lower one) the converter behaves as a constant current source [Moh89], providing an inherent overload protection capability together with the best output characteristic for a CCPS.

All of the above advantages are lost for $f_s > f_0/2$, while for f_s increasingly lower $f_0/2$ the average current supplied gets accordingly lower, thus increasing the capacitor charge time.

Operation of the SLR converter can be accurately simulated with MicroSim[1] (Figure 4.5) using actual component values and a supply voltage of 56 V (one tenth of the actual one, to facilitate convergence). The switches commutation sequence is as follows:

1. S1 and S4 close at time 0
2. S1 and S4 open at time $1 / (2\ f_0)$
3. Negative current flows back through D5 and D7, reaching zero at time $1 / f_0$
4. S3 and S2 close at time $k + 1 / f_0$
5. S3 and S2 open at time $k + 1 / f_0 + 1 / (2\ f_0)$
6. Negative current flows back through D6 and D8, reaching zero at time $k + 1 / f_0 + 1 / f_0$
7. The switching cycle is repeated

K is the dead time between phase 3 and phase 4: when $k = 0$ then $f_s = f_0/2$, while for $k > 0$ is $f_s < f_0/2$.

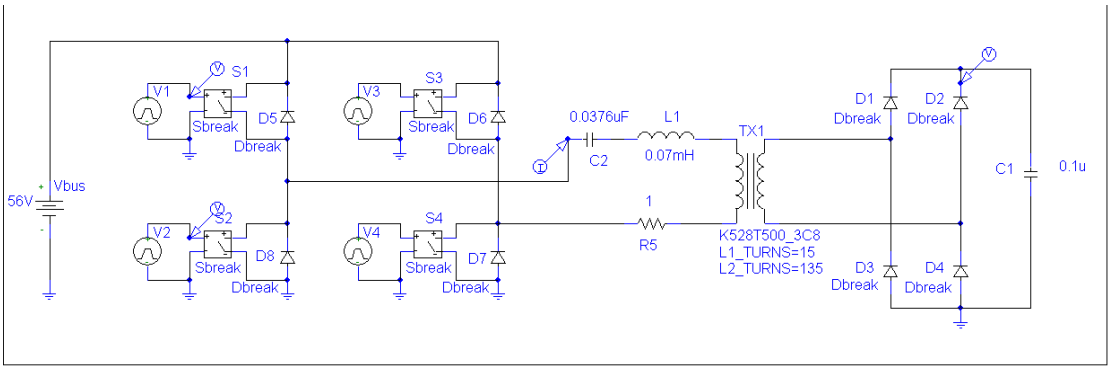

Figure 4.5 MicroSim simulation of the SLR converter.

With the component values used in the simulation $f_0 \approx 100$ kHz, $1/(2\ f_0) \approx 5$ µs and k is chosen to be zero. As it can be seen from the simulation results (Figure 4.6), the current flowing in the series-resonant load C2 and L1 is a series of sinusoids and the switches are commutated when the current crosses zero. Voltage on the capacitor under charge increases at a constant rate, as the pulsed charging current average value is constant during all the cycle.

The maximum peak reverse current flowing through the diodes when one switch pair is open is given by:

$$I_{OFF\max} = -\frac{V_{in}}{Z_0} \qquad \text{(Eq.5)}$$

[1] MicroSim was an original trademark of MicroSim Corporation, which merged with Orcad in 1998, which in turn recently merged with Cadence Corporation.

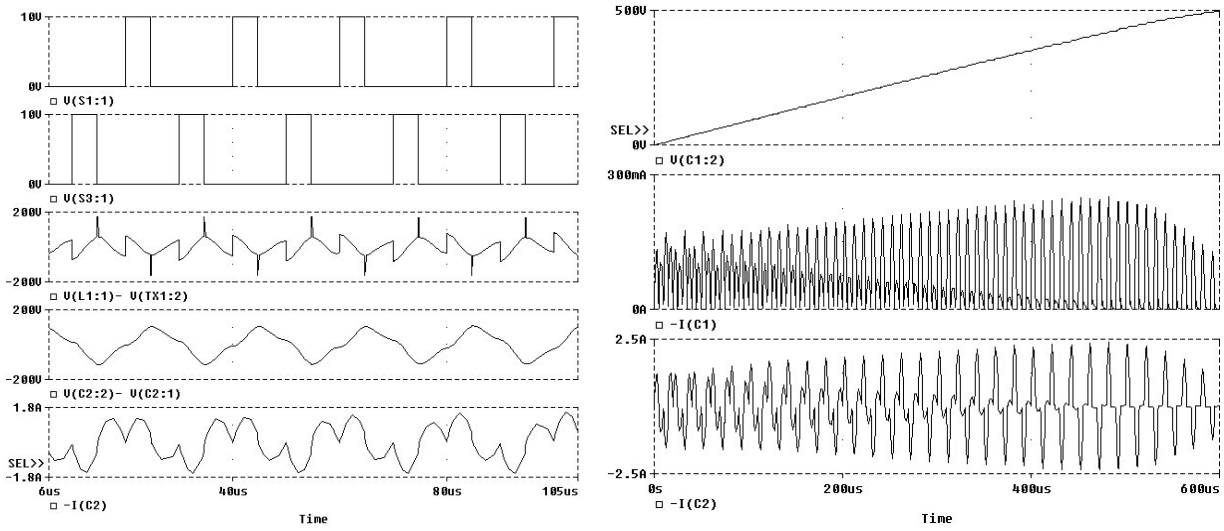

Figure 4.6 SLR converter simulation waveforms.

The previous value is assumed at the charge beginning and drops down to zero at the charge end: this is due to the voltage reversal effect across the load terminals, caused by the voltage present on the capacitor under charge. Conversely, the maximum peak current flowing in the load C2 and L1 when a switch pair is closed is given by:

$$I_{ON\max} = \frac{2V_{in}}{Z_0} = -2I_{OFF\max} \qquad \text{(Eq.6)}$$

This value is reached only at the end of the charge and is due to the energy accumulated in the resonant load C2 and L1: at charge beginning is $I_{ON} = -I_{OFFmax}$. Therefore, the SLR converter switches must be capable to stand I_{ONmax}, while the diodes can be sized to operate at I_{OFFmax} only. With the component values used in the simulation is:

$$I_{OFF\max} = -\frac{V_{in}}{Z_0} = -\frac{V_{in}}{\sqrt{\frac{L_1}{C_2}}} = \frac{56}{\sqrt{\frac{0.07\cdot 10^{-3}}{0.0376\cdot 10^{-6}}}} = -1.3\ \text{A} \qquad \text{(Eq.7)}$$

$$I_{ON\max} = -2I_{OFF\max} = 2.6\ \text{A} \qquad \text{(Eq.8)}$$

The RMS capacitor charging current can be calculated directly from the capacitor charging rate displayed in Figure 4.6 as:

$$I_{Crms} = \frac{C_1 \Delta V}{\Delta t} = \frac{0.1\cdot 10^{-6}\cdot 500}{600\cdot 10^{-6}} = 83.3\ \text{mA} \qquad \text{(Eq.9)}$$

The RMS current in the resonant load and transformer primary I_{1rms} can be calculated by balancing the average power between capacitor (P_{Cave}) and load (P_{Lave}):

$$P_{Cave} = \frac{I_{Crms}\cdot \Delta V}{2} = \frac{83.3\cdot 10^{-3}\cdot 500}{2} = 20.825\ \text{W} \qquad \text{(Eq.10)}$$

$$I_{1rms} = \frac{P_{Lave}}{V_{in}} = \frac{P_{Cave}}{V_{in}} = \frac{20.825}{56} = 372\ \text{mA} \qquad \text{(Eq.11)}$$

The theoretical power achieved with these component values is (taking into account that the simulation used one tenth of the actual supply voltage):

$$P = \frac{0.5 \cdot C_1 \cdot (\Delta V)^2}{\Delta t} = \frac{0.5 \cdot 0.1 \cdot 10^{-6} \cdot 5000^2}{600 \cdot 10^{-6}} = 2083 \text{ W} \qquad \text{(Eq.12)}$$

Considering now the actual supply voltage of 560 V, the expected current values can be calculated as:

$$I'_{Crms} = 10 \cdot I_{Crms} = 0.833 \text{ A}$$
$$I'_{1rms} = 10 \cdot I_{1rms} = 3.72 \text{ A}$$
$$I'_{ON\max} = 10 \cdot I_{ON\max} = 26 \text{ A}$$
$$\mathrm{I}'_{\mathrm{OFFmax}} = 10 \cdot I_{OFF\max} = 13 \text{ A}$$

5. CONVERTER DESIGN

The SLR converter includes a full-bridge switch, a linear power supply used to generate the 560 V DC initial voltage and galvanic isolation for the bridge control inputs.

5.1. Full-bridge switch

The converter full-bridge switch (Figure 5.7) uses four IGBTs type IRG4PH40UD, which feature an integrated anti-parallel diode with a relatively fast and soft reverse recovery characteristic. The IGBT is a relatively new power semiconductor device, which provides the best features of both the MOSFET and the BJT [Tak95]. Among its advantages:

- Low-power, voltage-driven gate turn-on and turn-off. Gate impedance as high as a MOSFET.
- Low conduction losses.
- Positive temperature coefficient. The device will not experience thermal run-away typical of BJTs.
- Possibility to use either integrated or external anti-parallel diode.

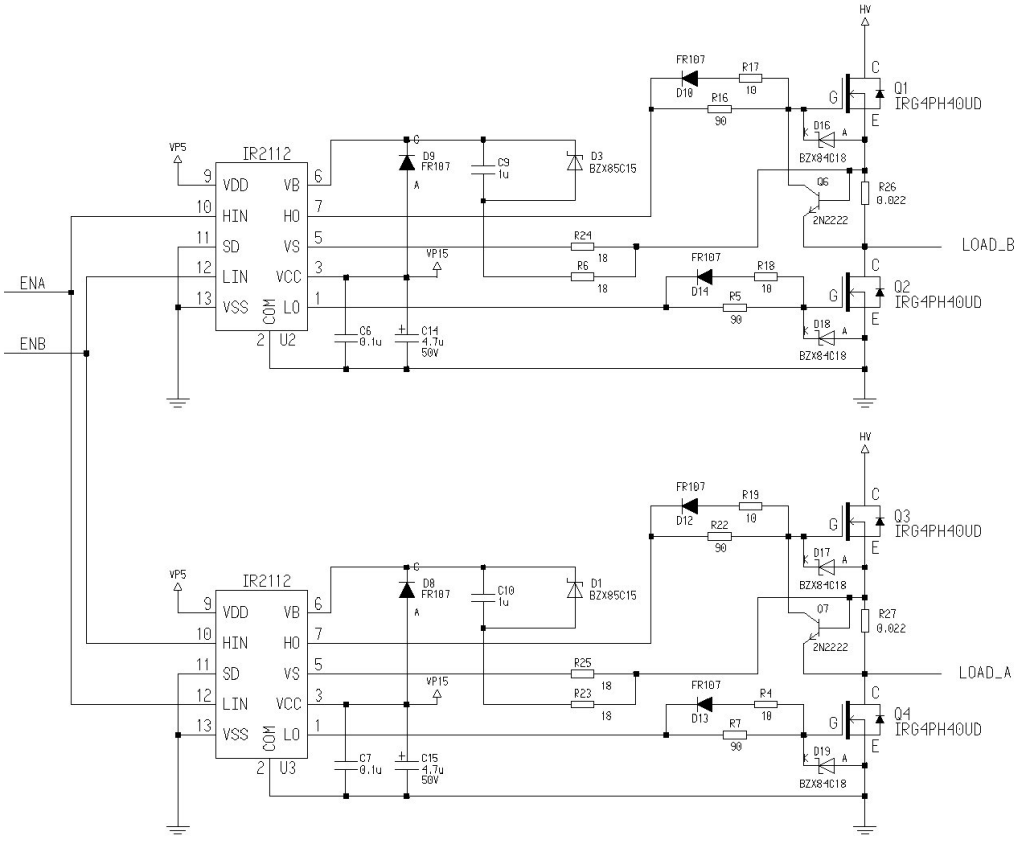

Figure 5.7 Converter full-bridge schematic diagram.

The major disadvantage of the IGBT is its slow turn-off speed that results in the well-known current tail: as the SLR converter commutations take place always when the load current is zero, the slow turn-off doesn't represent a problem. The manufacturer recommends the IRG4PH40UD for hard-switching operation up to 40 kHz, but for resonant-mode operation 200 kHz functionality is guaranteed.

Parameter	Value
Collector-to-Emitter breakdown voltage	1200 V
Continuous collector current	30 A
Pulsed collector current	120 A
Diode continuous forward current	8 A
Diode maximum forward current	130 A

Table 1 Absolute maximum ratings for the IRG4PH40UD device.

The four IGBT gate drive requirements are easily fulfilled by two IR2112 driver ICs. The IR2112 (Figure 5.8) has got TTL/CMOS compatible inputs and Schmitt trigger buffers with hysteresis equal to 10% of VDD. The signals from the input logic are coupled to the individual channels through high noise immunity level translators. This allows the ground reference of the logic supply (VSS on pin 13) to swing by ±5V with respect to the power ground (COM). This feature is of great help in coping with the less than ideal ground layout of a typical power conditioning circuit. As a further measure of noise immunity, a pulse-width discriminator screens out pulses that are shorter than 50ns or so.

The output stage is implemented with two N-Channel MOSFETs in totem pole which can sink (source) gate currents up to 420 mA (200 mA). The source of the lower driver is independently brought out to pin 2 (COM) so that a direct connection can be made to the source of the power device for the return of the gate drive current. An undervoltage lockout prevents the outputs from operating if VCC is below the specified value (typically 8.6/8.2V).

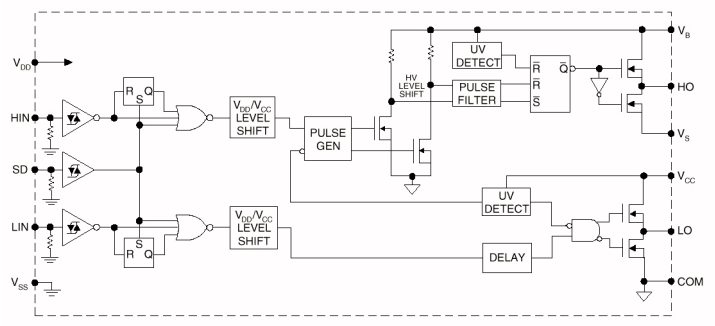

Figure 5.8 Block diagram of the IR2112.

The high side driver is capable of floating from 600V to -5V with respect to power ground (COM). Its input commands have to be level-shifted from the level of COM to whatever potential VS is floating at, which can be as high as 500V. The on/off commands are transmitted in the form of narrow pulses at the rising and falling edges of the input command. They are latched by a set/reset flip-flop referenced to the floating potential. The use of pulses greatly reduces the power dissipation associated with the level translation: a pulse discriminator filters the set/reset pulses from fast dv/dt transients appearing on the VS node.

The high side channel has its own undervoltage lockout which blocks the gate drive if the voltage between VB and VS , i.e., the voltage across the upper totem pole is below its limits (typically 8.7/8.3V). The high voltage level translator circuit is designed to function properly even when the VS node swings below the COM pin by 5V. This can occur due to the forward recovery of the lower power diode or to the Ldi/dt induced voltage transient (see Section 7.6).

In order to operate the bridge in the SLR converter mode, signal ENA enables Q6 and Q4 while signal ENB enables Q2 and Q3. The gate charge for the high side IGBT is provided by a bootstrap capacitor (C9 and C10) which is charged by the 15V supply through the bootstrap diode (D8 and D9) during the time when the device is off (and the low side IGBT is turned on). Zeners D3 and D1 together with resistors R6 and R23 prevent C9 and C10 to overcharge as a result of ground bounce.

5.2. Linear power supply

The 560 V DC (HV in Figure 5.7) is derived by rectifying the 3-phase mains and filtered by two 470 µF 400 V electrolytic capacitors (Figure 5.9). R11 is a NTC surge protector responsible for decreasing the current peak generated at power-on when the capacitors are not yet charged. The capacitor pair terminals cannot be connected to the mains neutral pole, and the converter ground cannot be heartened. All the bridge switch circuitry is subjected to potentials ranging from +400 V to –400 V in respect to the neutral pole and special measurement techniques must be employed, including insulation transformers and differential probes.

U1 provides 15 V to the IR2112, needed to drive the IGBT gates, while U5 generates the 5V required by the TTL logic onboard. LED D5 signals the presence of the 560V voltage while LED D6 lights when transformer T1 is powered: this is useful as the high-voltage and the low-voltage sections of the linear power supply can be powered separately for safety reasons.

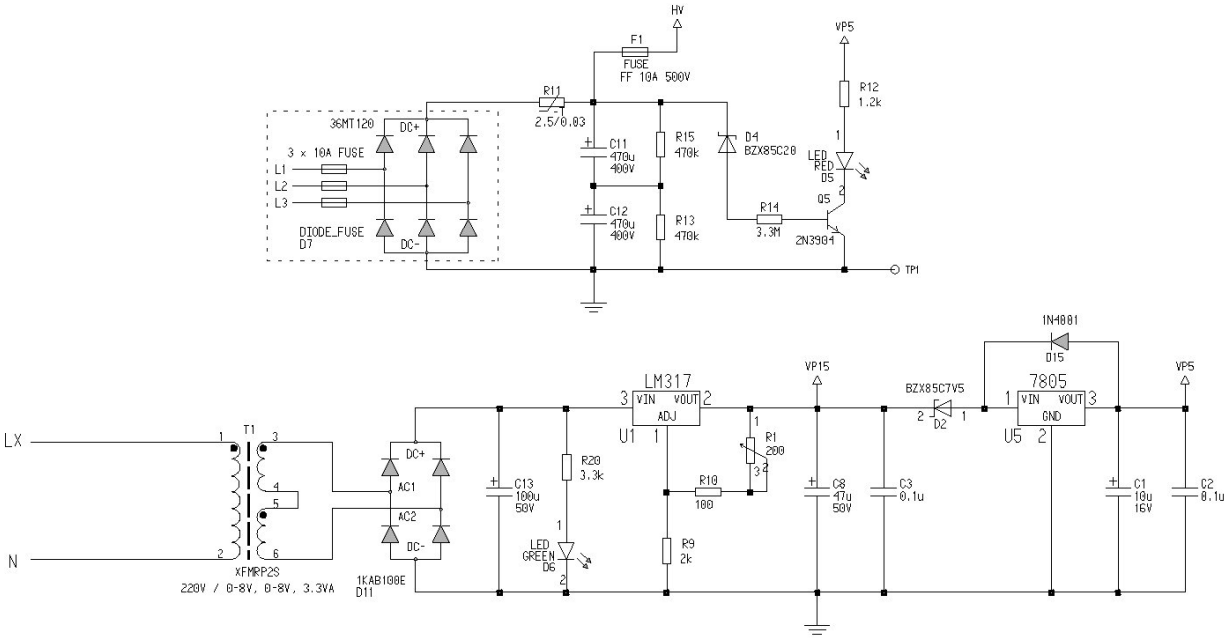

Figure 5.9 Converter linear power supply schematic diagram.

5.3. Converter control inputs

Galvanic isolation at the two bridge control inputs is provided by the HCPL-2430 high-speed logic optocoupler U4 (see Figure 5.10), followed by a tiny logic block built around U6 that ensures signals ENA and ENB can never be asserted simultaneously. This would result in the bridge switch short-circuiting directly HV to ground with catastrophic consequences.

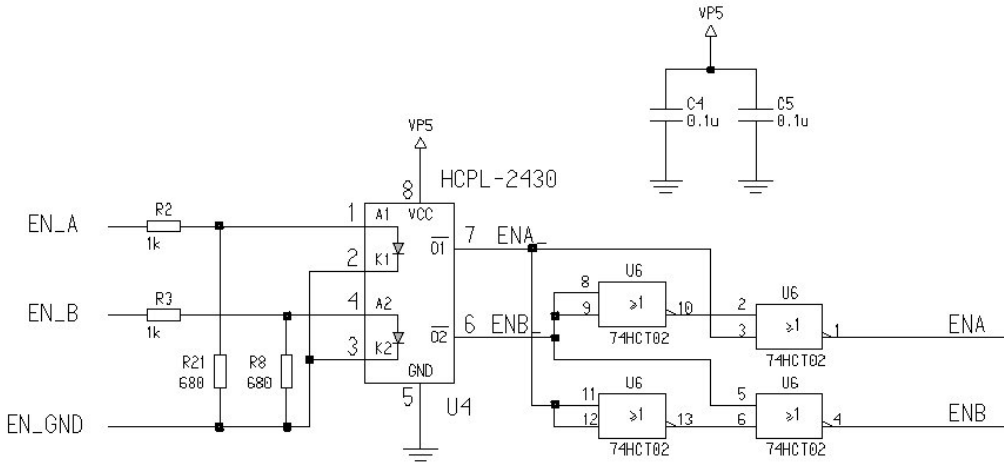

Figure 5.10 Converter control inputs schematic diagram.

6. RESONANT LOAD DESIGN

The resonant load includes the capacitor C (Figure 4.4), the step-up transformer, and a high-voltage, full-wave rectifier bridge. Each arm of the full-wave rectifier bridge is composed by a series of five BYM36G diodes (Figure 6.11), capable to stand a continuous reverse voltage of 1400 V and an average forward current of 2.9 A. Each bridge arm is therefore functional up to 7 kV, ensuring a sufficient margin for transients. Due to the relatively high frequency of the pulses to be rectified (100 kHz), a fast rectifier is required to avoid overheating: the BYM36 provides a reverse recovery time of max 250 ns, which is sufficient to fulfil the requirements.

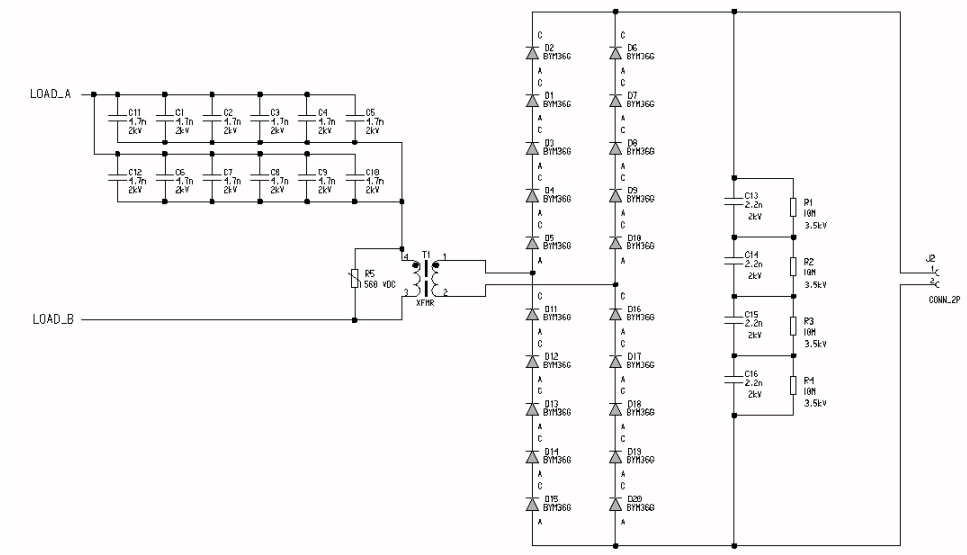

Figure 6.11 Resonant load schematics.

The bridge DC output is shunted by a light load composed by C13 to C16 and R1 to R4: this facilitates an homogenous voltage distribution when more converters are connected in series to reach a 20 kV output voltage. R5 is a 560 V varistor meant to protect the converter circuitry from voltage transients coming through the transformer secondary to its primary winding. C1 to C4 are not assembled: their pads can be used to fine-tune the load resonant frequency.

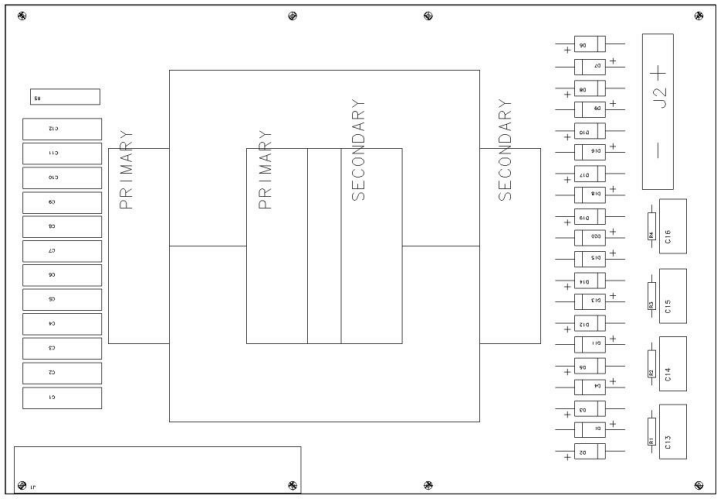

Figure 6.12 Resonant load PCB assembly.

The leakage inductance of the transformer is utilized as the resonance inductor L. The transformer primary is composed of 3 windings of 15 turns each connected in parallel to minimize skin effect losses: wire section is 0.5 mm. The secondary has got a single winding of 135 turns of wire with section 0.3 mm: as the wire is wound on a single layer, there are no inter-winding corona discharges. Due to the relatively lousy coupling of primary and secondary, the primary exhibits a winding inductance of 0.7 mH and a leakage inductance of 70 μH, as required.

The transformer uses two U-shaped ferrite cores type U100/57/25-3C90 (Philips) having a square cross-section and characteristics as from Table 2. The assembled transformer measures 100 x 114 x 25 mm.

Symbol	**Parameter**	**Value**
V_e	Effective volume	199000 mm^2
A_e	Effective cross section	6.45 cm^2
A_w	Window area	30 cm^2
A_L	Inductance factor	5500 nH
μ_e	Effective permeability	2200

Table 2 Characteristics of the U100/57/25-3C90 core.

7. PROBLEMS ENCOUNTERED AND SOLUTIONS

Even if the IGBT commutations take place at zero current, unwanted spikes and noise in general are present in many nodes of the schematics, due to:

- Parasitic capacities C_{ce}, C_{gc} and C_{ge} internal to the IGBTs.
- PCB traces impedance.
- Reverse recovery time of the anti-parallel diodes.
- Electromagnetic radiation and coupling within the converter PCB.

The most significant source of unwanted noise is, anyway, the Tesla transformer itself: when the spark gap conducts and the charged capacitor is quickly discharged on the primary coil, high voltage transients are generated on the capacitor. These transients propagate through the step-up transformer as a sudden change of load impedance, which in turn causes high-current spikes in the IGBT bridge.

The most challenging part of the SLR converter design was the elimination of these disturbances that caused permanent damage of the IGBTs and of their IR2112 driver IC. A first set of problems was encountered when charging a test capacitor bank: after these where fixed, a new set of fault conditions showed up when the SLR converter was used together with the Tesla transformer. This required another problem-analysis iteration in order to protect properly the converter from the severe transients generated.

This activity required a considerable amount of time and effort, plus a thorough analysis of several manufacturers application notes and design information bulletins. In the following sections each of the fault sources is identified and the solution leading to their elimination is described.

7.1. Rapid di/dt

The commutation of each IGBT caused noise glitches on the 15V and 5V supply voltages, and also on the ENA and ENB drive signals. This affected the IGBT driver IC operation so much that the switching was unstable and sometimes oscillating. More, the turn-off of the low side IGBT caused a negative spike on node A (see Figure 7.18). A too rapid switching speed was supposed to be the cause of this problem: on the other hand, a fast commutation wasn't needed as in the SLR topology it was performed at zero current.

In order to reduce switching noise and to be sure not to run into avalanche breakdown [Mit95] or stray inductance problems (see Section 7.2), it was decided to reduce the di/dt rate. Increasing the value of the gate series resistor, the amplitude of the negative spike decreases rapidly, while the turn-off time increases linearly [Bax96].

The resistors between the driver IC and the IGBT gates were increased to 90 ohms (R16, R5, R22 and R7 in Figure 5.7): this change effectively reduced the measured glitches and eliminated totally switching instability.

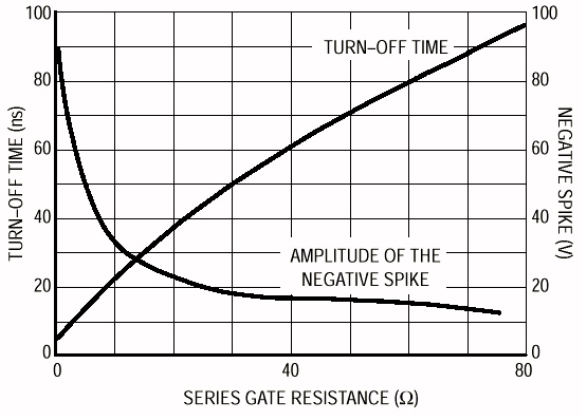

Figure 7.13 Series gate resistance vs. spike amplitude and turn-off time as measured on the test board used in [Bax96.]

7.2. Stray inductance

The "common emitter inductance" [Int990] is the inductance that is in common to the collector-emitter (i.e. load) current path and to the gate-emitter (i.e. gate drive) path (Figure 7.14): it is the sum of the IGBT package inductance and the PCB trace stray inductance. This inductance creates a feedback path from the collector circuit to the gate circuit that is proportional to $L \cdot \frac{dI_c}{dt}$. When the high-side IGBT turns on, this voltage subtracts from the applied gate voltage slowing down the switching. Much more dangerous is its effect when the low-side turns on: then the generated voltage adds to the applied high-side IGBT gate voltage.

In the SLR converter case, IGBT commutation is deliberately slowed down and load current follows a smooth sinusoidal profile: therefore, no significant voltage should be generated by the common emitter inductance. The presence of transients, instead, makes a change to this ideal situation.

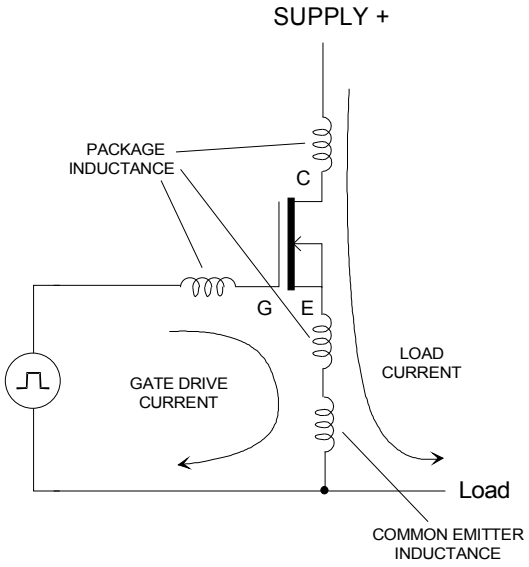

Figure 7.14 Common emitter inductance in the high-side IGBT.

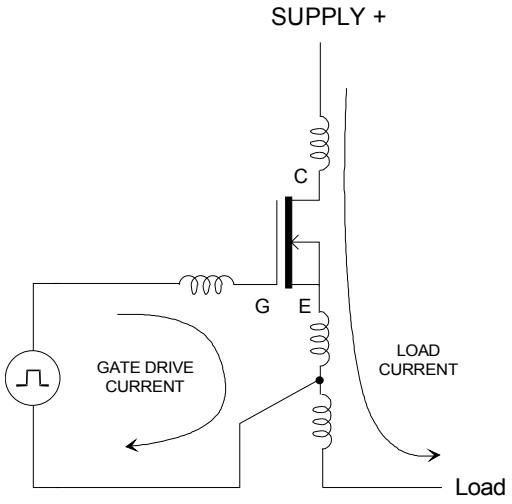

Figure 7.15 Solution that eliminated the common emitter inductance feedback.

The measured transients consisted in random and abrupt load current changes, with typical rise times of 5 - 10 ns: even a 20 nH of stray inductance could have easily generated 10 – 20 V that could have turned on the high-side IGBT creating a short-circuit. This mechanism was seen very clearly as noise superimposed to the gate charge voltage: as this noise was actually capable of turning on and off the IGBT, this event generated a higher supply current spike that, in turn, reinforced the gate transient that originated the whole event chain.

This problem was eliminated by a careful PCB trace routing: the gate drive return trace connects directly to the IGBT emitter terminal, while a separate, wider trace connects also to the same point but is used to carry the emitter and load current only (Figure 7.15).

7.3. Bridge current protection

In some faulty situation, two IGBTs on the same full-bridge side got into conduction simultaneously, thus connecting the 560 V HV potential (Figure 5.7) to ground. Even if fuse F1 (Figure 5.9) is capable of opening within 1 ms time, the charge present in C11 and C12 vaporized large section of the wide PCB traces, interrupting the current path and leaving the fuse intact. After this event the converter PCB was so much damaged that it couldn't be repaired.

To eliminate the catastrophic consequences of the overcurrent (not its causes) transistors Q6 and Q7 were added, together with R26 and R27. These resistors are thick-film, low-inductance, surface mount type: when their voltage drop reaches about 0.7 V, Q6 and Q7 start conducting and therefore clip the IGBTs V_{ge}. This limits the maximum current in each of the bridge arms to 33 A and gives time to the fuse to safely blow open, avoiding damages to PCB.

7.4. "Shoot-through" current

The IGBT has got considerable junction capacitance between all its terminals (Figure 7.16). When the high-side switch is off and the relative low-side switch turns on, the high-side will see a positive-going voltage applied to its collector and emitter terminals. Assuming a relatively high drive source impedance, this voltage change will be reflected as a positive-going voltage transient across the gate and emitter terminals, in the approximate ratio of [Int936]:

$$\frac{\Delta V_{ge}}{\Delta V_{ce}} = \frac{C_{cg}}{C_{cg} + C_{ge}} = \frac{C_{res}}{C_{ies}} \qquad \text{(Eq.13)}$$

The above capacitance ratio goes from about 1/2 to 1/7 (Figure 7.17): this means that a positive transient generated in this way can easily turn on the high-side IGBT. As it goes into conduction it clamps the V_{ce} that is causing it to conduct so that the gate voltage never goes much beyond its threshold. The end result is a high current transient called "shoot-through" current and increased power dissipation.

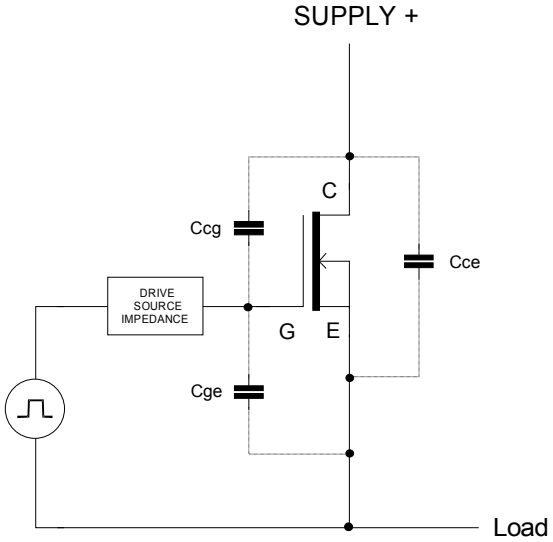

Figure 7.16 IGBT internal capacitances (high-side switch).

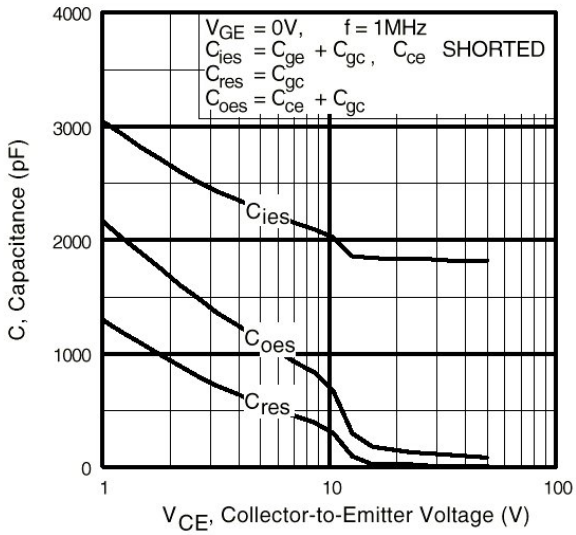

Figure 7.17 Internal capacitance vs. Vce for the IRG4PH40UD IGBT.

On the contrary, a negative-going ΔV_{ce} (e.g. when the low-side IGBT is tuning off) will not be clamped: the voltage transient ΔV_{ge} produced may exceed the gate voltage rating causing permanent damage in the device. To reduce the risk of shoot-through, the drive source impedance must be made low enough: this will limit the gate-source voltage rise and also prevent spurious turn-on [Int936, Int937 and Int990].

Shoot-through current was actually observed on the SLR converter even with no load. As the gate drive impedance was to be reduced still without decreasing the turn-on time, a series of a 10 ohm resistor with a fast diode was added in parallel to the 90 ohm gate drive resistor (D10, D14, D12, D13, R17, R18, R19 and R4 in Figure 5.7). These components clamped the gate voltage when the IGBT was in off state and effectively eliminated the problem.

7.5. Driver IC bootstrap overvoltage

The IR2112 IGBT driver IC uses voltage V_{bs} to charge the gate of the high-side IGBT Q1 (Figure 7.18): this supply sits on top of the VS voltage (node A), which oscillates between GND and HV. V_{bs} is derived as follows: when Q2 turns on, node A is pulled down to ground and the bootstrap capacitor charges through the bootstrap diode from the VCC supply. Then, when Q1 needs to turn on, the boostrap capacitor can feed its gate with the stored charge. V_{bs} needs to be between 10 and 20 V to ensure that the IGBT can be fully enhanced.

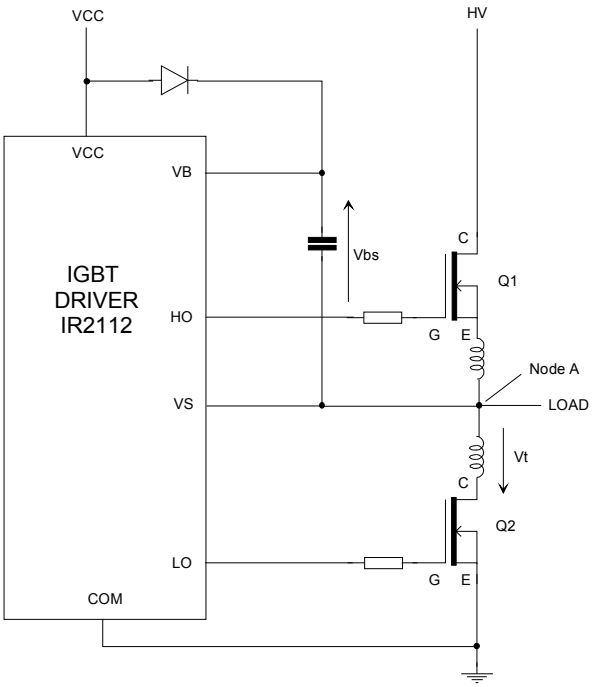

Figure 7.18 IGBT driver bootstrap circuitry.

Problems arise if node A goes below ground, due to the voltage V_t developed in the stray inductance. Then the bootstrap capacitor overcharges to a voltage V_{bs} = VCC + V_t: if this voltage reaches 25 V, a diode internal to the IR2112 can experience breakdown and the IC can enter latch-up. In turn, latch-up can easily drive both IGBT into conduction state thus producing a IGBT failure [Ir973].

The SLR converter experienced failures that resulted from simultaneous conduction of both high-side and low-side IGBTs: glitches over 25 V were measured on V_{bs}, indicating the possibility of driving the IR2112 into latch-up. Initially a 15 V zener diode was added in parallel to the bootstrap capacitor (D1 and D3 in Figure 5.7): this removed the slower glitches but still left a considerable amount of them.

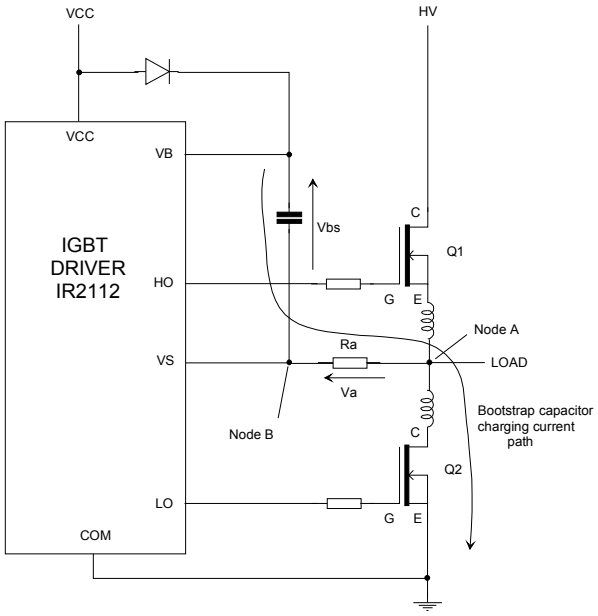

Figure 7.19 Attempt to reduce Vbs overvoltage by insertion of resistor Ra.

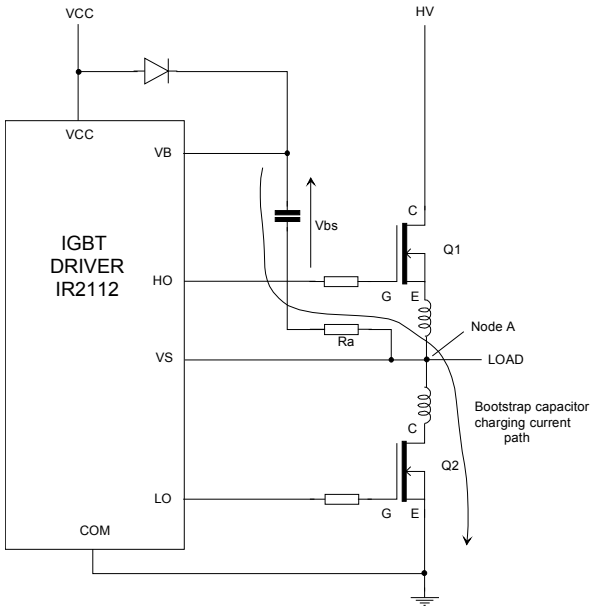

Figure 7.20 A better alternative for reducing Vbs overvoltage by insertion of resistor Ra.

The following modification was to add resistor Ra between node A and node B as shown in Figure 7.19 and suggested in [Ir973] and [Bax96]: Ra needed to be rised to a value of 18 ohm in order to properly eliminate all glitches on V_{bs}. But, as Ra was also connected in series to the IR2112 pin VS, this modification resulted in shoot-through: the bootstrap capacitor charging voltage created a positive voltage drop Va on Ra that tended to turn on the high-side IGBT. Therefore, Ra was moved as shown in Figure 7.20: this solution removed the V_{bs} overvoltage problem and also avoided shoot-through induced by bootstrap charging.

7.6. Driver IC VS undershoot

While the failure resulting from an overvoltage on V_{bs} had been eliminated (see previous section), the undershooting at node A was still present and measurable: the high and low-side IGBT were still sometimes driven on simultaneously.

If the IR2112 pin VS (i.e. node A) undershoot exceeds 5V, a mechanism internal to the IC will temporarily latch the high side output in its current state and will not respond to input transitions (on the high-side) while the undershoot persists [Ir973]. Clearly, activating the low-side input at that time would result in contemporary excitation of both IGBTs: this was believed to be the fault mechanism.

Because the stray inductance had already been minimized and the dv/dt rate reduced properly (see previous sections), the only possible care left was to add a resistor Rb between pin VS and note A to limit the current into pin VS [Bax96]. The resulting connection (Figure 7.21) did actually prevent the IGBT simultaneous conduction, the V_{bs} overcharge and also shoot-through.

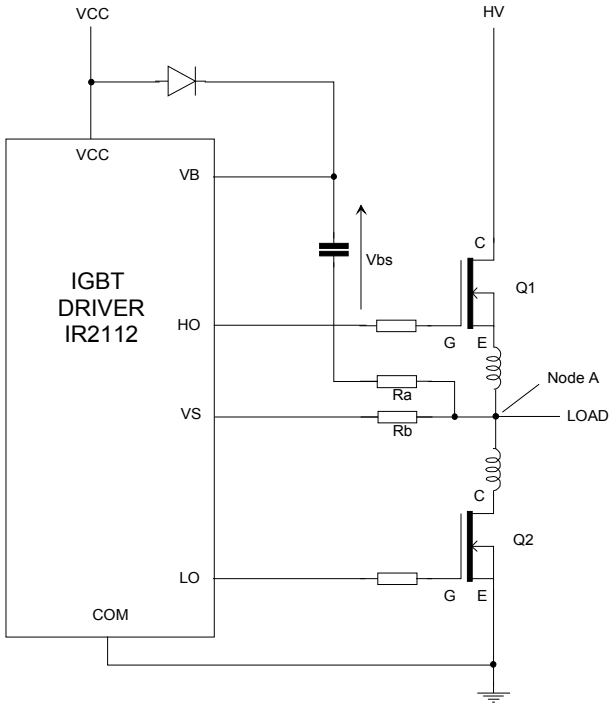

Figure 7.21 Optimal protection solution: Ra prevents overvoltage on Vbs while Rb limts the current on pin VS suppressing negative spikes.

7.7. IGBT gate overvoltage

When the SLR converter begun to be used together with the Tesla transformer, it became exposed to much more serious, asynchronous transients coming from the spark gap short circuiting the charged capacitor and the converter output (Figure 2.1). The bridge IGBTs where failing quite often with gate, emitter and collector shorted all together: the manufacturer failure analysis pointed out that the cause of the failure was a breakdown of the gate junction.

As the IGBT maximum allowed gate to emitter voltage is 20V, the gate charge voltage (VCC in Figure 7.21) was

reduced from the original 18V to 15V, to provide a greater noise margin. As well, zener diodes were added between gate and emitter, in order to clamp all spikes exceeding 18V (D16, D17, D18 and D19 in Figure 5.7). The zeners are SMD type and are placed very close to the IGBT terminals to minimize parasitic inductances and decrease response time. This modification put a stop to the IGBT failures.

7.8. Asynchronous converter drive

The SLR converter is driven by a controller board that generates the bridge signals EN_A and EN_B (Figure 5.10) with the timing described in Section 4: the controller measures the charged capacitor voltage and interrupts the drive pulse train when the target voltage is reached. Momentary charge interruptions can also happen in the middle of the cycle, due to the transients measured on the capacitor that cannot be completely filtered. There is in fact a tradeoff between low-pass filtering this feedback signal and still keeping a slew-rate suitable for following the charge profile.

Both genuine and temporary charge interruptions actually shut-down the controller EN_A and EN_B outputs, while subsequent charge continuation restarted a new output timing sequence. From the resonant load point of view, this resulted in randomly shortened and lengthened bridge conduction cycles that violated the timing required to achieve zero current switching. The wrong timing produced high-current spikes in the resonant load that damaged the IGBTs and the IR2112 drivers.

The controller board logic was modified so that:

1. The currently undergoing cycle (EN_A or EN_B enabled) will complete before the drive is suspended.
2. When the charge is restarted, the first output to be enabled will be always different from the one enabled last (e.g. if EN_A was enabled last, a new cycle will begin with enabling EN_B)

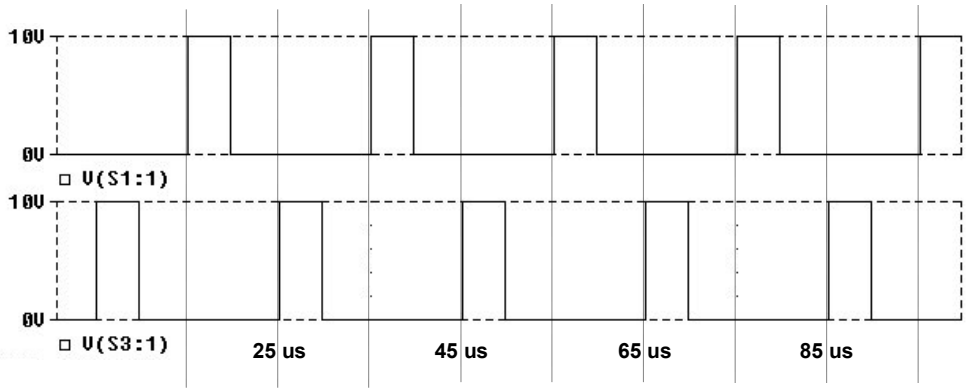

Figure 7.22 SLR converter EN_A and EN_B correct drive timing. The sequence can be safely interrupted only in correspondence of the vertical dotted markers.

This ensured that the converter drive cycle could be interrupted only at the time instants described in Figure 7.22 and would always restart in a consistent manner. This practice avoided the generation of high-current spikes due to chaotic commutation, and the consequent IGBT and IR2112 failures.

8. ASSEMBLY AND MECHANICS

The power converter is assembled on a double-side PCB sized 100 x 160 mm and enclosed in a standard 19" rack plug-in frame box, measuring 3U x 14HP. Connections to the other modules are realized through DIN 41612 type H connectors.

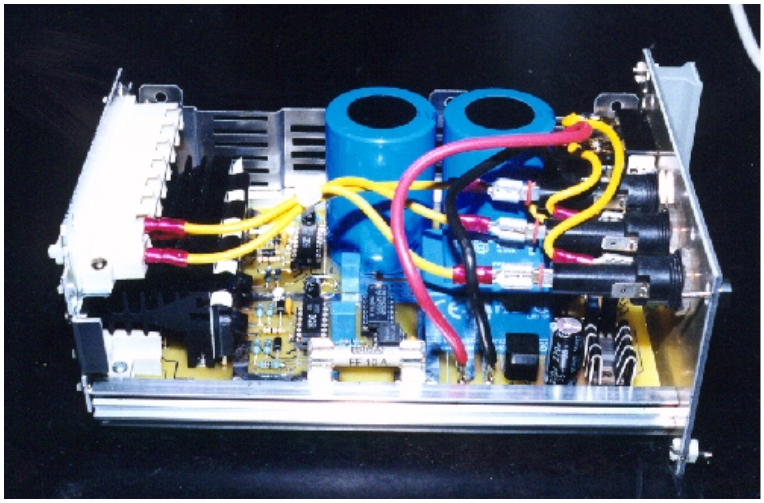

Figure 8.23 The SLR converter assembled in its plug-in frame.

As the commutation losses of the SLR topology are very low, the converter modules' IGBT are equipped with a relatively small heatsink (3.7 ˚C/W) which has proven to be sufficient. The three-phase mains has shown to be prone to flashover with the rest of the converter circuitry, due to its floating nature and the potential swinging effect of the Tesla transformer transients. The mains are therefore taken to the module through a second DIN connector different from the one used by the rest of the signals and fed to the PCB only after rectification.

All of the resonant load components are assembled on a double-side PCB sized 160 x 232 mm and mounted on a standard rack plug-in frame, measuring 6U x 14HP. The high voltage terminals from the diode bridge are connected to high voltage connector sockets mounted on the module front panel. These connector sockets and their relative plugs have been developed at the HUT High Voltage Laboratory and tested to be functional up to 30 kV DC.

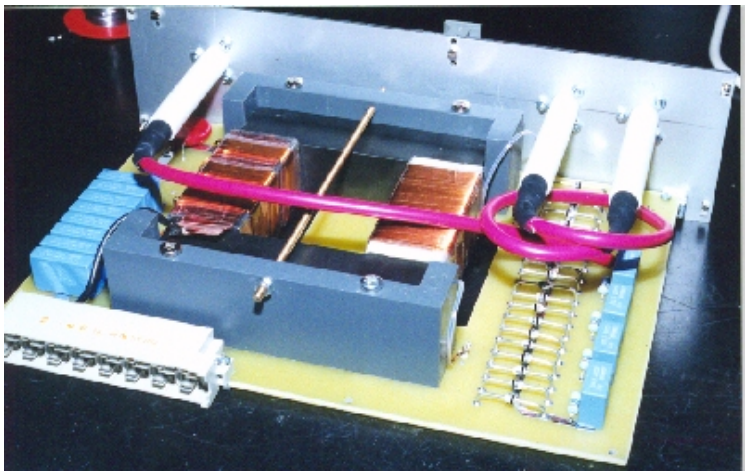

Figure 8.24 The resonant load assembled in its plug-in frame.

9. CONCLUSION

A solid-state resonant power converter developing a power of 2 kW and a maximum voltage of 5 kV has been designed and built successfully using off-the-self components. The series-loaded resonant topology choice resulted in:

- minimized switching losses
- reduced size of the heatsink required
- snubbers were not needed at all
- relatively slow components like IGBTs could be used as switching devices, even at a switching frequency of 100 kHz.
- constant current output behavior, with intrinsic overload protection.

Filtering and a careful PCB layout have proven to be crucial for the apparatus to withstand the severe transients it is exposed to:

- inductance of the PCB traces connecting to the IGBTs must be kept at a minimum
- two separate ground (power and digital ground) must be used and connected together in a single point
- the IGBT gate charge voltage must be low enough so that possible transients will not drive V_{ge} over 20V, damaging the device.

To avoid the generation of high current peaks and the consequent injection of noise into other components it is mandatory to drive the converter bridge with the correct timing and phase. Timing within a switching cycle must always be according to the resonant load requirement: 5 μs on, 5 μs off, then 5 μs reversed and finally 5 μs off. Repetition rate of these cycles can be varied (decreased) as needed with the effect of slowing down the capacitor charge rate.

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11. DEFINITIONS, ACRONYMS AND ABBREVIATIONS

BJT	Bipolar Junction Transistor
CCPS	Capacitor Charging Power Supply
IC	Integrated Circuit
IGBT	Insulated Gate Bipolar Transistor
HUT	Helsinki University of Technology
HV	High Voltage
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
OPAMP	Operational Amplifier
PCB	Printed Circuit Board
SMD	Surface Mounting Device